REMARKS

Claims 1-7 remain in the application. Claims 4-7 are subject to a restriction requirement and are currently non-elected claims and stand withdrawn. Claim 1 has been amended to more clearly define Applicant's invention. Claims 1-3 remain in the application as elected claims.

Claims 1-3 have been rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's Admitted Prior Art (hereinafter referred to as "APA"), the Examiner referring to Applicant's Fig. 4.

Claim 1 has been amended. Claim 1 recites a semiconductor device comprising: a substrate layer comprising a first dopant density; an epitaxial layer comprising a second dopant density formed on the substrate layer; and a semiconductor switch formed on the epitaxial layer, wherein the semiconductor switch comprises an active region and a termination region of the semiconductor device; wherein the substrate and epitaxial layers are formed so as to provide a uniform thickness throughout the active and termination regions, and wherein the epitaxial layer is formed so that a first thickness of the epitaxial layer in the active region is less than a second thickness of the epitaxial layer in a termination region formed peripherally to the active region enabling the on-resistance of the semiconductor switch to be reduced without necessarily increasing the breakdown voltage of the semiconductor switch, and/or the breakdown voltage of the semiconductor switch to be increased without necessarily increasing the on-resistance of the semiconductor switch.

Referring to Applicant's Fig. 4, the epitaxial layer 23 of the device 21 is trenched and the gate 25 is recessed to reduce the JFET pinch resistance and improve the channel packing density. In devices 20 and 21, the breakdown voltage of the device may be lowered by the increased exposure of the gate to the epitaxial region defined by each of the thicknesses T_{B2} and T_{B3}. The thickness of the device 21 in the active and termination regions is thus not uniform because of the trench formed to receive the gate 25, clearly different from the claim 1 limitation of requiring a uniform thickness, and formed for a different reason from the claim limitation of enabling the on-resistance of the semiconductor switch to be reduced without necessarily increasing the breakdown

voltage of the semiconductor switch, and/or the breakdown voltage of the semiconductor switch to be increased without necessarily increasing the on-resistance of the semiconductor switch.

It is clear therefore, that claims 1-3 are different from the Fig. 4 structure shown and described in the present application. An early and favorable action thereon is therefore earnestly solicited. The Examiner is encouraged to call the undersigned attorney to resolve any unresolved issues in the present application.

In connection with the foregoing matter, please charge any additional fees which may due, or credit any overpayment, to Deposit Account Number 50-1133.

Respectfully submitted,
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